



Ehong Technology Co.,Ltd

# **QCA4020 Module (WL501)**

## **Product Specification**

WL501

October 31, 2018

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# Revision history

Revision	Date	Description
A	October 2018	Initial release

# Contents

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<b>1 Introduction</b>	<b>5</b>
<b>2 Hardware specification</b>	<b>7</b>
2.1 WL501 module pinout	7
2.2 WL501 interface summary	12
2.3 Bootstrap signals	13
2.4 Electrical characteristics	13
2.4.1 General DC electrical characteristics	13
2.4.2 WL501 2.4 GHz power measurements	14
2.4.3 WL501 5 GHz power measurements	14
2.4.4 BLE power measurements	15
2.4.5 15.4 power measurements	15
<b>3 Mechanical interface specification</b>	<b>16</b>
3.1 WL501 module dimensions	16

## Figures

Figure 1-1 WL501 block diagram	5
Figure 2-1 WL501 front view	7
Figure 2-2 WL501 back view	8
Figure 2-3 WL501 pinout definition	9
Figure 3-1 WL501 module dimensions	16
Figure 3-2 WL501 module pinout dimensions (in mm)	17
Figure 3-3 WL501 module pinout dimensions-Detail B (in mm)	18

## Tables

Table 2-1 WL501 module non-GPIO pinout definition	9
Table 2-2 WL501 module pinout definition and QCA4024 GPIO assignment	10
Table 2-3 Bootstrap mode	13
Table 2-4 JTAG mode	13
Table 2-5 XTAL mode	13
Table 2-6 32.768KHz Sleep Clock Mode	13
Table 2-7 DC electrical characteristics for digital I/Os	14
Table 2-8 2.4 GHz power measurements at antenna port at 25 C, 3.3V nominal	14
Table 2-9 5 GHz power measurements at antenna port at 25 C, 3.3V nominal	14
Table 2-10 BLE power measurements at antenna port at 25 C, 3.3V nominal with external PA	15
Table 2-11 15.4 power measurements at antenna port at 25 C, 3.3V nominal with external PA	15

# 1 Introduction

The WL501 module provides a highly-integrated and flexible platform for developing and evaluating products and applications based on the QCA4020 SoC. The WL501 module can be either used with CDB20 development kit for software development or incorporated into OEM products to enable rapid deployment of Wi-Fi connected systems.

The WL501 module includes the following components:

- QCA4020 chip (WLAN/BLE/15.4)
- A printed antenna
- 32 Mb NOR flash memory

The QCA4020 is a dual band 1x1 802.11 a/b/g/n device optimized for low-power embedded applications with single-stream capability for both Tx and Rx. It has an integrated network processor with a large set of TCP/IP with IPv4/IPv6-based services.

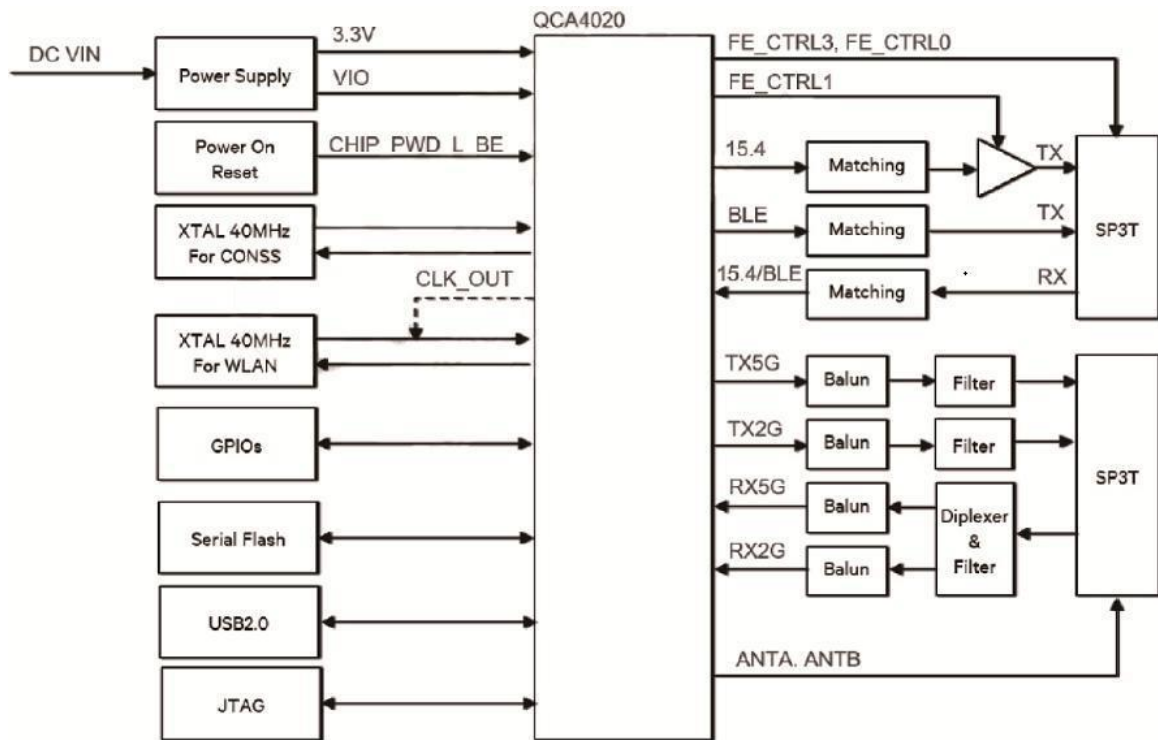


Figure 1-1 WL501 block diagram

## WL501 module features

- Dual-Band IEEE 802.11 a/b/g/n, single stream 1x1
- BLE 5.0
- ZigBee 15.4
- Green Tx power saving mode
- Low -power listen mode
- Four-layer PCB design
- Rich set of GPIO(s) and interfaces: I2C, HSUART, UART, SPI, QSPI, SDIO 2.0, I2S, JTAG, Sensor ADC (up to 8 channels, 12bit, 1Msps). Up to 8 PWM optimized for LED lighting applications.
- Secure boot and support for application-level AES encryption and image authentication hash function (SHA256)
- Advancement power management scheme to minimize power dissipation for each use case

## WL501 manufacturing interface

- USB 2.0 interface with integrated controller and PHY for manufacturing test and configuration

## WL501 host interfaces

- UART host interface to a remote microcontroller with an AT style command set

# 2 Hardware specification

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## 2.1 WL501 module pinout



Figure 2-1 WL501 front view

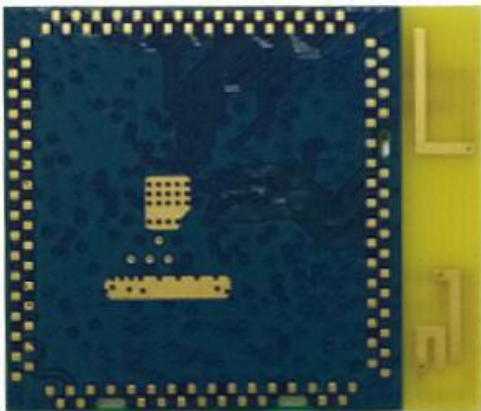


Figure 2-2 WL501 back view

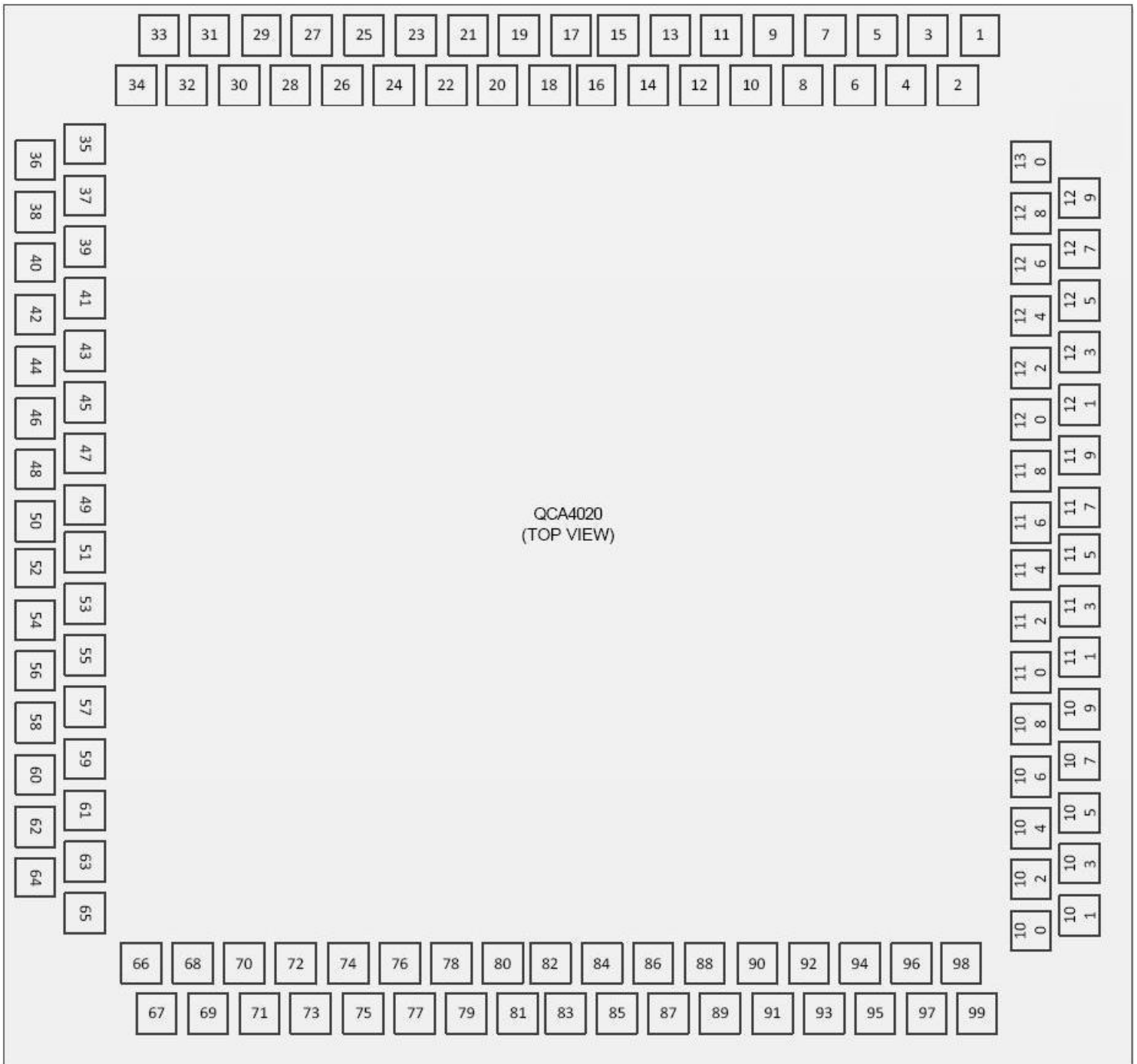


Figure 2-3 WL501 pinout definition



Table 2-1 WL501 module non-GPIO pinout definition

Pin #	Pin Name	Description
<b>Power</b>		
2-4	VBATT_BE	3.3V Input Power
<b>Input Signals</b>		
22	USB20_DM_BE	USB Differential Negative
23	USB20_DP_BE	USB Differential Positive

Pin #	Pin Name	Description
27	SENSEADC_0_BE	12bit ADC, ADC 0 input
24	SENSEADC_1_BE	12bit ADC, ADC 1 input
37	CHIP_PWD_L_BE	BLE/15.4 Reset Pin
<b>Ground</b>		
1, 5, 33, 38, 42, 45, 67-69, 71, 76, 85, 98-101, 104, 109, 111, 115, 119, 124, 127, 130	GND	Ground
<b>No Connect</b>		
43,44	VDDIO18_BE	Not used, NC
39-41	VDD11_SWREG_OUT	Not used, NC
128, 129	VDDIO18_WL	Not used, NC
117	PWRDWN_OUT_N	Not used, NC
17	BYPASS_INT_PMU_MSK	Not used, NC
126	IOT_MODE_EN_WL	Not used, NC
7	WAKEUP_N	Not used, NC
13	USB_DPOS	USB Differential Positive, WLAN interface, Not used, NC
14	USB_DNEG	USB Differential Negative, WLAN interface, Not used, NC

Table 2-2 WL501 module pinout definition and QCA4024 GPIO assignment

Pin #	Pin Name	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	PTA	Codec
84	GPIO4_BE	WL_WKUP_BE								
83	GPIO5_BE	GPIO_5							BT_ACTIVE	
81	GPIO6_BE	GPIO_6							WLAN_ACTIVE	
79	GPIO7_BE	GPIO_7							BT_PRIORITY	
61	GPIO8_BE	GPIO_8				M0&M4_UART0_RX	JTAG1_BE_TCK			
58	GPIO9_BE	GPIO_9				M0&M4_UART0_TX	JTAG1_BE_TDO			
59	GPIO10_BE	GPIO_10	I2C0_Master_SCL				JTAG1_BE_TMS			
56	GPIO11_BE	GPIO_11	I2C0_Master_DA				JTAG1_BE_TDI			
32	GPIO12_BE	GPIO_12						pwm_out_0		

Pin #	Pin Name	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	PTA	Codec
54	GPIO1_3_BE	GPIO_13						pwm_out_7		
52	GPIO1_4_BE	GPIO_14				HS_UART0_DM_CTS				
55	GPIO1_5_BE	GPIO_15				HS_UART0_DM_TXD				
53	GPIO1_6_BE	SPI0_CS2_N	I2C1_Master_SCL			HS_UART0_DM_RFR			BT_ACTIVE	
51	GPIO1_7_BE	SPI0_CS1_N	I2C1_Master_SDA			HS_UART0_DM_RXD			WLAN_ACTIVE	
16	GPIO1_8_BE	GPIO_18	SPI_Slave_CLK	SDIO_Slave_CLK	SD_Master_CLK (O)	HS_UART1_DM_CTS		pwm_out_6		
11	GPIO1_9_BE	GPIO_19	SPI_Slave_CS_N	SDIO_Slave_CMD	SD_Master_CMD (B)	HS_UART1_DM_TXD		pwm_out_1		
15	GPIO2_0_BE	GPIO_20	SPI_SLAVE_MISO	SDIO_Slave_DATA_0	SD_Master_DATA_0 (B)	HS_UART1_DM_RXD		pwm_out_2		
19	GPIO2_1_BE	GPIO_21		SDIO_Slave_DATA_1	SD_Master_DATA_1 (B)			pwm_out_4		
26	GPIO2_2_BE	GPIO_22		SDIO_Slave_DATA_2	SD_Master_DATA_2 (B)			pwm_out_3		
21	GPIO2_3_BE	GPIO_23	SPI_SLAVE_MOSI	SDIO_Slave_DATA_3	SD_Master_DATA_3 (B)	HS_UART1_DM_RFR		pwm_out_5		
29	GPIO2_4_BE	GPIO_24	SPI0_Master_CS_N			M0&M4_UART2_RX	JTAG2_BE_TCK			
31	GPIO2_5_BE	GPIO_25	SPI0_Master_CLK			M0&M4_UART2_TX	JTAG2_BE_TDO			
28	GPIO2_6_BE	GPIO_26	SPI0_Master_MOSI				JTAG2_BE_TMS			
30	GPIO2_7_BE	GPIO_27	SPI0_Master_MISO				JTAG2_BE_TDI			
46	GPIO2_8_BE	GPIO_28								I2S_BCLK
47	GPIO2_9_BE	GPIO_29								I2S_RXD
48	GPIO3_0_BE	GPIO_30								I2S_TXD
50	GPIO3_1_BE	GPIO_31								I2S_FSYNC

Pin #	Pin Name	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	PTA	Codec
49	GPIO3_2_BE	GPIO_32								I2S_MCLK
10	GPIO3_3_BE	CHIP_PWD_L_WL								
80	GPIO4_1_BE	PWR_STATUS								
57	GPIO4_8_BE	Ext_32K_IN								
64	GPIO4_9_BE	GPIO_49								
78	GPIO5_0_BE	GPIO_50					JTAG3_BE_TCK			
63	GPIO5_1_BE	GPIO_51					JTAG3_BE_TDO			
62	GPIO5_2_BE	GPIO_52					JTAG3_BE_TMS			
60	GPIO5_3_BE	GPIO_53					JTAG3_BE_TDI			
25	GPIO5_4_BE	GPIO_54						SENSEADC_2		
20	GPIO5_5_BE	GPIO_55						SENSEADC_3		
18	GPIO5_6_BE	GPIO_56						SENSEADC_4		
12	GPIO5_7_BE	GPIO_57						SENSEADC_5		
9	GPIO5_8_BE	GPIO_58						SENSEADC_6		
8	GPIO5_9_BE	GPIO_59				HS_UART2_DM_CTS (I)		SENSEADC_7		
82	GPIO6_0_BE	GPIO_60				HS_UART2_DM_TXD (O)			BT_PRIORITY	

## 2.2 WL501 interface summary

- 2x I2C Master Interface
- 1x High speed UART
- Up to 3Mbps data rate
- 1x UART
- Up to 115200 kbps data rate

- 1x I2S
- 1x JTAG
- 1x ADC Sense
- 1x USB2.0 interface
- 1x SPI Interface

## 2.3 Bootstrap signals

Table 2-3 Bootstrap mode

GPIO9_BE	GPIO22_BE	Description
0	0	Force M4 to load image from flash memory (Default)
0	1	Force M4 to boot in EDL (Emergency Download Mode).

Table 2-4 JTAG mode

GPIO9_BE	GPIO25_BE	GPIO18_BE	Description
0	0	0	No JTAG enabled
0	0	1	JTAG Pins on GPIO[53:50]_BE
0	1	0	JTAG Pins on GPIO[11:8]_BE
0	1	1	JTAG Pins on GPIO[27:24]_BE
1	X	X	Not Allowed

Table 2-5 XTAL mode

GPIO23_BE	Description
0	40MHz Xtal
1	Not Allowed

Table 2-6 32.768KHz Sleep Clock Mode

GPIO21_BE	GPIO20_BE	Description
0	0	Chip Internal LPO
0	1	External Crystal 32.768KHz
1	0	External 32.768KHz TCXO Clock connected to GPIO_48_BE
1	1	Not Allowed

## 2.4 Electrical characteristics

### 2.4.1 General DC electrical characteristics

These conditions apply to all DC characteristics unless otherwise specified:  $T_{amb} = 25\text{ C}$ ,

$V_{BATT\ BE} = 3.3\text{ V}$

Table 2-7 DC electrical characteristics for digital I/Os

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	High level I voltage	–	2.4	–	3.6	V
V <sub>IL</sub>	Low level I voltage	–	-0.3	–	0.3	V
V <sub>OH</sub>	High level O voltage	–	3.0	–	3.3	V
V <sub>OL</sub>	Low level O voltage	–	-0.3	–	0.4	V

## 2.4.2 WL501 2.4 GHz power measurements

Table 2-8 2.4 GHz power measurements at antenna port at 25 °C, 3.3V nominal

Standard	Modulation	Index	Typical Tx Compliant Power <sup>1</sup>	Rx Sensitivity	Unit
802.11b	BPSK	1 Mbps	17	-94	dBm
	QPSK	2 Mbps	17	-91.5	dBm
	CCK	5.5 Mbps	17	n/a	dBm
	CCK	11 Mbps	17	-87	dBm
802.11g	BPSK	6Mbps	17	-91.5	dBm
	64 QAM	54Mbps	13	-75	dBm
802.11n HT20	BPSK	MCS0_40	17	-92	dBm
	64 QAM	MCS7_20	12	-71.5	dBm
802.11n HT40	BPSK	MCS0_40	14	-89.5	dBm
	64 QAM	MCS7_40	11	-69.5	dBm

## 2.4.3 WL501 5 GHz power measurements

Table 2-9 5 GHz power measurements at antenna port at 25 °C, 3.3V nominal

Standard	Modulation	Index	Typical Tx Compliant Power <sup>2</sup>	Rx Sensitivity	Unit
802.11a	BPSK	6 Mbps	12	-89.5	dBm
	64 QAM	54 Mbps	7	-72.5	dBm
802.11n HT20	BPSK	MCS0_20	11	-89.5	dBm
	64 QAM	MCS7_20	6	-69.5	dBm
802.11n HT40	BPSK	MCS0_40	11	-86.5	dBm
	64 QAM	MCS7_40	5	-65	dBm

<sup>1</sup> Numbers shown based on OLPC per board calibration

<sup>2</sup> Numbers shown based on OLPC per board calibration

## 2.4.4 BLE power measurements

**Table 2-10 BLE power measurements at antenna port at 25 C, 3.3V nominal with external PA**

Parameter	Description	Typical	Unit
Tx Power	BT LE 1M	7	dBm
	BT LE 2M	7	dBm
Rx Sensitivity	BT LE 1M	-93	dBm
	BT LE 2M	-93	dBm

## 2.4.5 15.4 power measurements

**Table 2-11 15.4 power measurements at antenna port at 25 C, 3.3V nominal with external PA**

Parameter	Description	Typical	Unit
Tx power	O-QPSK DSSS	17	dBm
Rx Sensitivity	O-QPSK DSSS	-101	dBm

# 3 Mechanical interface specification

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## 3.1 WL501 module dimensions

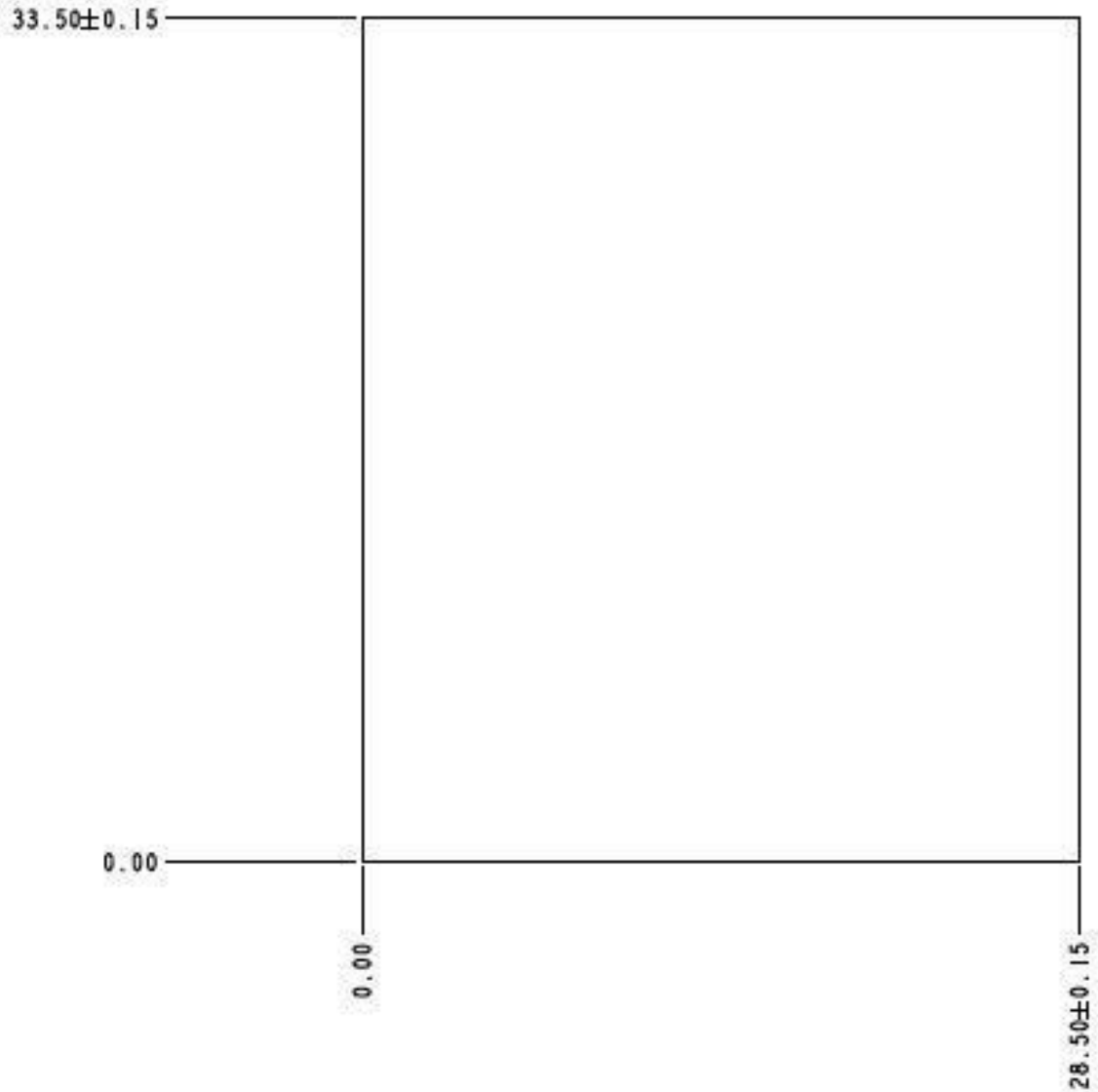


Figure 3-1 WL501 module dimensions



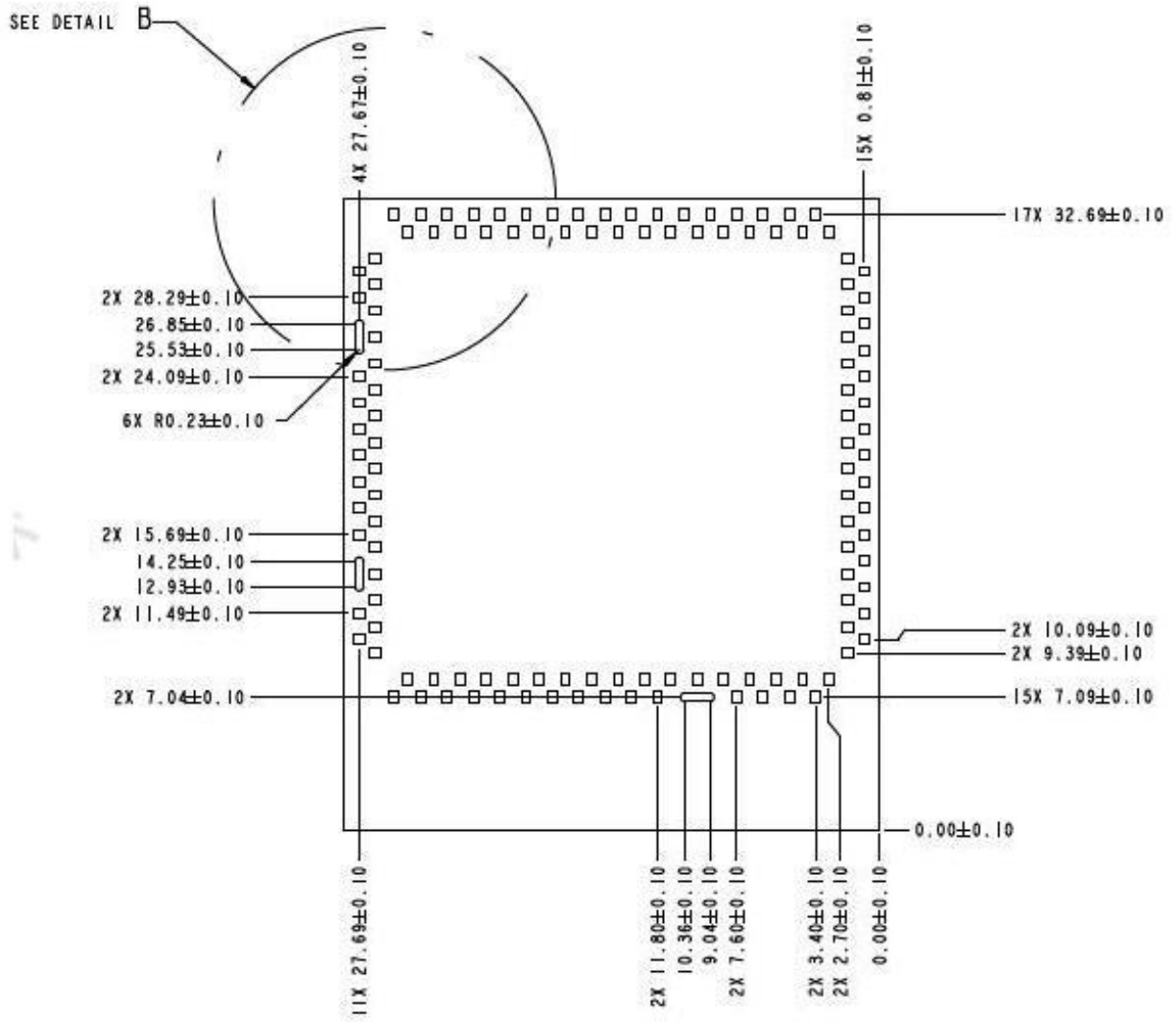


Figure 3-2 WL501 module pinout dimensions (in mm)

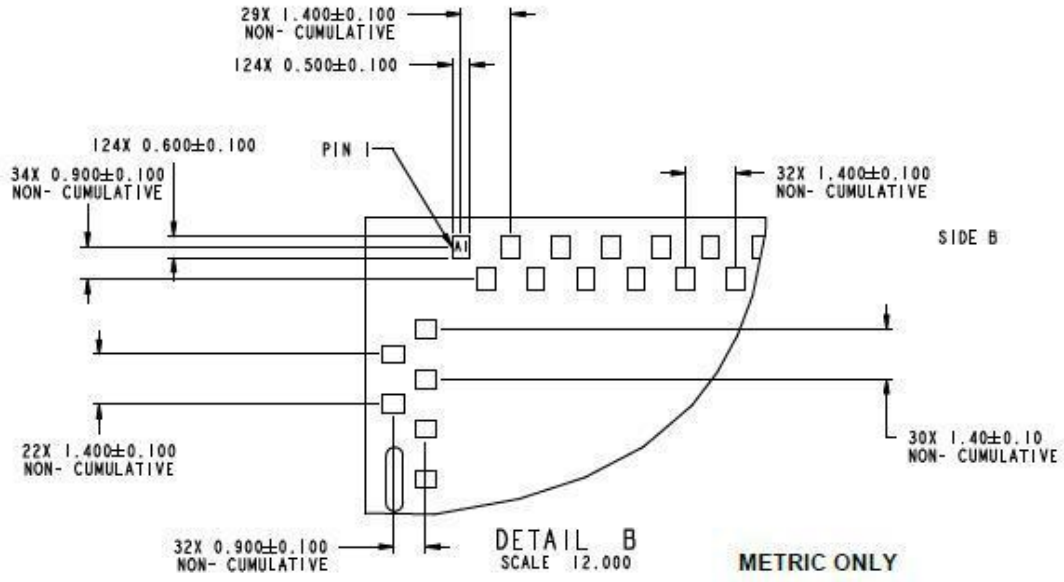


Figure 3-3 WL501 module pinout dimensions-Detail B (in mm)