EQM100-5

Datasheet

V1.0

Table of Contents

1 Product Overview

Powered by Qualcomm QCC711, EQM100-5 modules are purposely-designed M.2 Type 1216 soldered-down form factor BLE modules that combine multi-core processing capabilities, high-security as well as BLE long-range to cater to the demands of diverse IoT applications. Their compact size and on-chip memory of SRAM and RRAM (NVM) contribute to reduced costs and enhanced performance, making them an attractive choice for space-constrained IoT edge devices.

Unlike many other BLE modules on the market, EQM100-5 modules have integrated three processors – 64MHz Arm Cortex-M processor for application and 32MHz Arm Conrtex-M0 processor for BLE with shared on-chip memory of 128KB SRAM and 512KB RRAM. Additional Root-of-Trust 32MHz RISC-V processor with its own secure SRAM and ROM is dedicated to security subsystem to ensure the highest level of security for IoT applications with critical security needs. They have built-in resistive RAM (RRAM), the industry latest Non-volatile Memory (NVM) technology, eliminating need for externally attached NOR flash as well as resulting in more streamlined and cost-effective system. They also feature 3-wire and 4-wire SPI display control, making them capable of driving external LCD/TFT screens commonly found on a dedicated MCU. Furthermore, EQM100-5 modules can be powered directly by a battery, making it suitable for portable and battery-operated devices.

EQM100-5 can operate in hostless mode, capable of running both the Bluetooth stack and applications internally without requiring an external MCU. Moreover, they support hostless mode (HCI) through a UART interface, functioning as a Bluetooth transceiver to offload the Bluetooth stack. This enables the external MCU to focus on handling applications rather than managing the Bluetooth stack.

EQM100-5 modules have undergone rigorous regulatory compliance testing and are certified with FCC, CE, IC, UKCA, RCM, MIC, KC, SRRC and environmentally compliant with RoHS and WEEE directives. They also hold Bluetooth SIG 5.3 certification and will be software upgradable to SIG 5.4, ensuring seamless interoperability with other Bluetooth devices.

EQM100-5 modules include the following configuration in the table:

Module	Form Factor	Antenna
EQM100-5U	12 x 16 x 2.1 mm, 2.00 mm pitch, 76-pin, LGA	U.FL Antenna
EQM100-5B	12 x 20 x 2.1 mm, 2.00 mm pitch, 76-pin, LGA	PCB Antenna

EQM100-5 modules are graphically illustrated below:

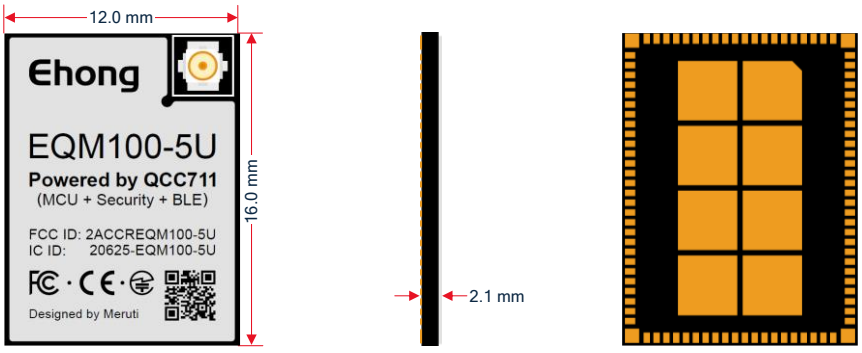

Figure 1: EQM100-5U Module View

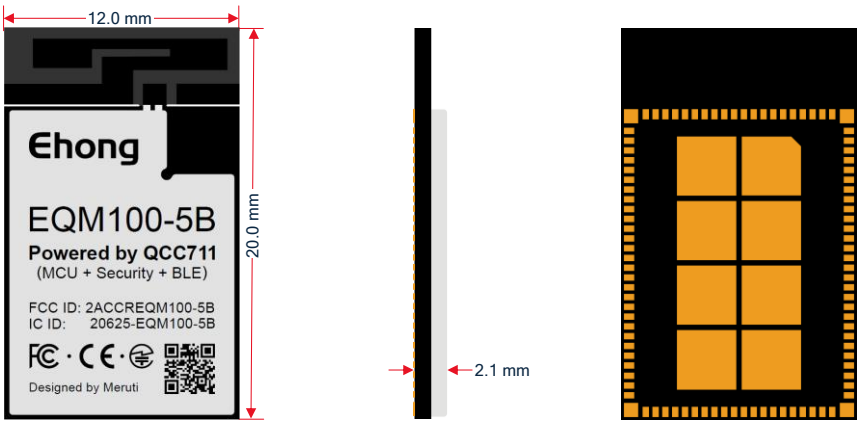

Figure 2: EQM100-5B Module View

The module specific development kits are also provided to facilitate application software development as shown below:

Figure 3: EQM100-5U Module Development Kit

Figure 4: EQM100-5B Module Development Kit

2 Hardware Specification

This section provides detailed hardware design and specification of EQM100-5 modules. The module hardware design has been optimized for small footprint and reduced RBOM cost.

2.1 Block Diagram

EQM100-5 integrates 2/4/8MB 2x3 8-USON NOR flash and 32.768kHz RTC crystal as stuffing options. The design also supports PCB antenna (EQM100-5B) or simply provides antenna pin (EQM100-5U) to allow customized antenna implementation on motherboard. The block diagram is shown below.

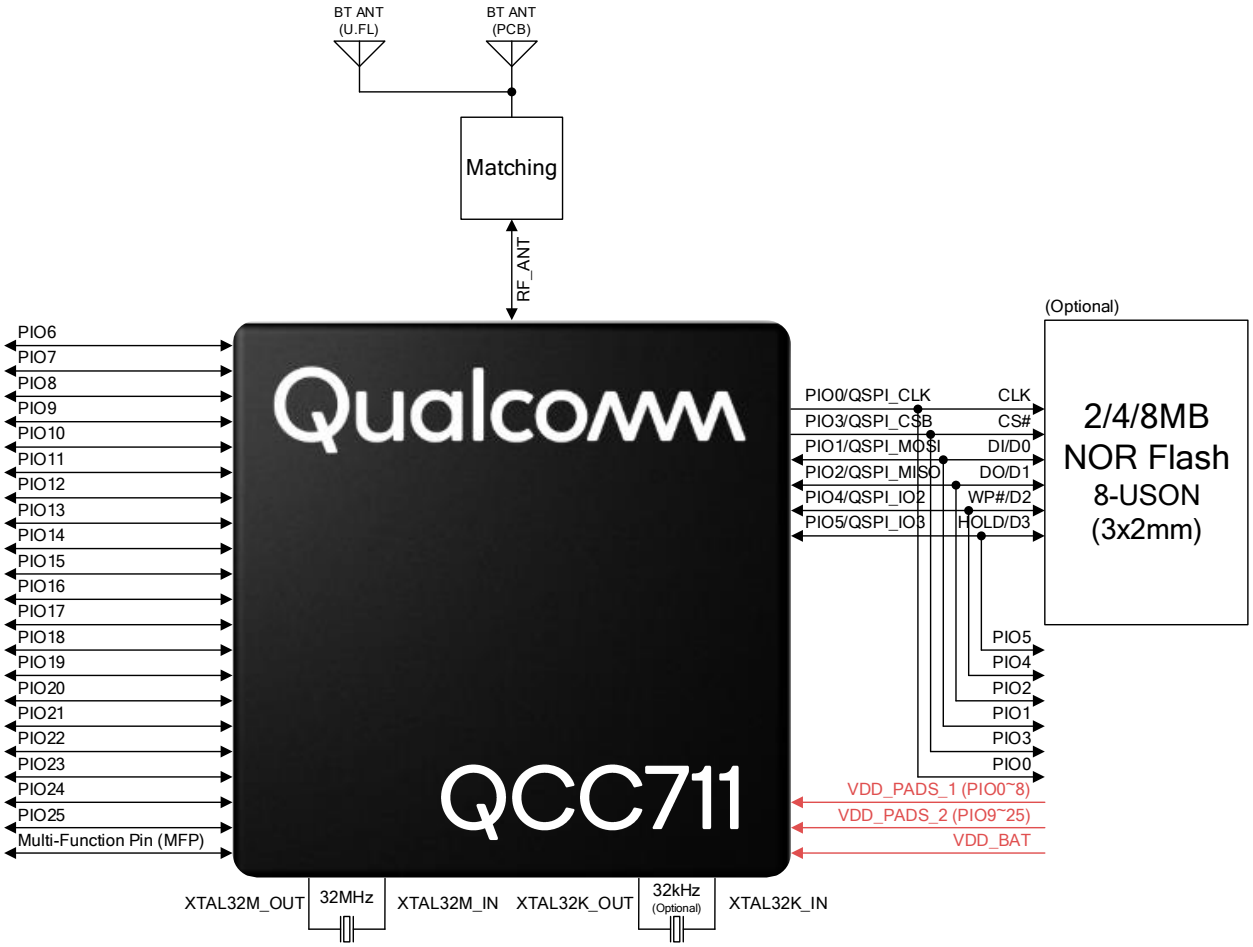

Figure 5: EQM100-5 Module Block Diagram

2.2 Pinout Description

2.2.1 Pin Map

EQM100-5U and EQM100-5B share the same pin map as illustrated below:

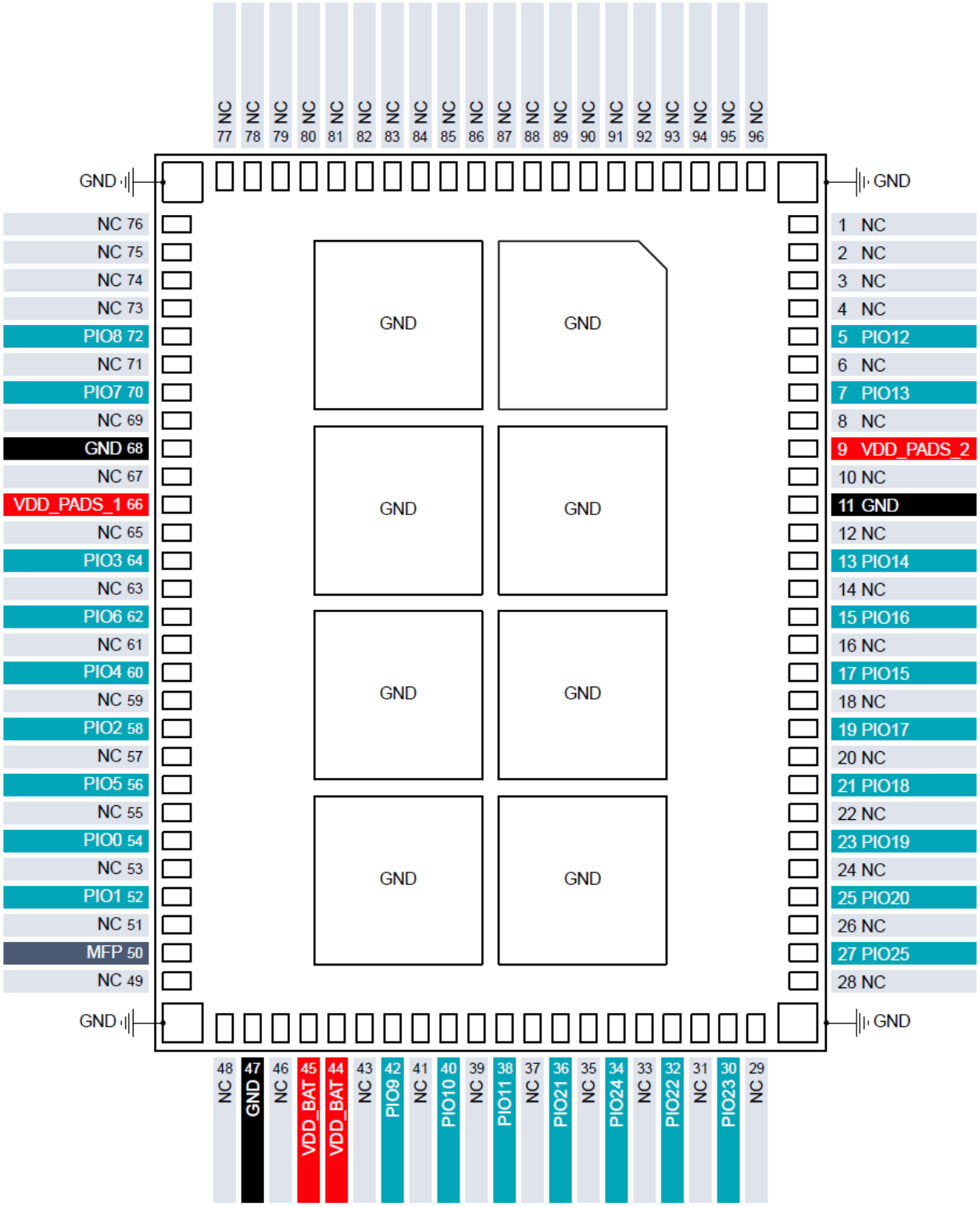

Figure 6: EQM100-5U Module Pin Map

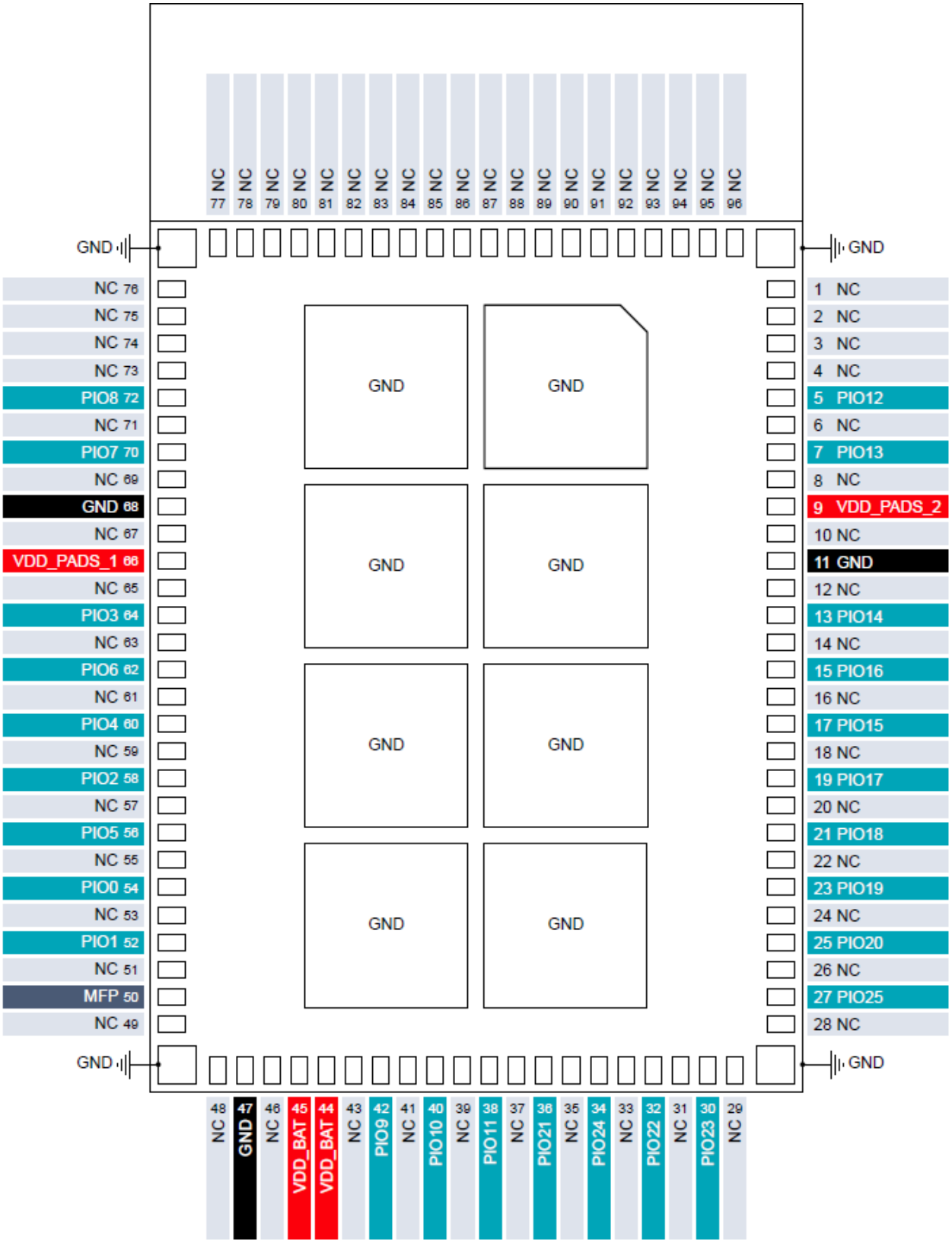

Figure 7: EQM100-5B Module Pin Map

2.2.2 Pin Definition

Pin	Pin Name	Type	Power Domain	Description
44,45	VDD_VBAT	PWR	-	Power input (1.71~3.6V)
66	VDD_PADS_1	PWR	I/O	Host I/O voltage input (≤ VDD_VBAT)
9	VDD_PADS_2	PWR	I/O	Host I/O voltage input (≤ VDD_VBAT)
11,47,68	GND	GND	GND	Ground
50	MFP	DI	VDD_VBATT	SW configurable as a reset input
54	PIO0	DI/DO	VDD_PADS_1	Generic PIO
52	PIO1	DI/DO	VDD_PADS_1	Generic PIO
64	PIO2	DI/DO	VDD_PADS_1	Generic PIO
56	PIO3	DI/DO	VDD_PADS_1	Generic PIO
60	PIO4	DI/DO	VDD_PADS_1	Generic PIO
56	PIO5	DI/DO	VDD_PADS_1	Generic PIO
62	PIO6	DI/DO	VDD_PADS_1	Generic PIO
70	PIO7	DI/DO	VDD_PADS_1	Generic PIO
72	PIO8	DI/DO	VDD_PADS_1	Generic PIO
42	PIO9	DI/DO	VDD_PADS_2	Generic PIO
40	PIO10	DI/DO	VDD_PADS_2	Generic PIO
38	PIO11	DI/DO	VDD_PADS_2	Generic PIO
5	PIO12	DI/DO	VDD_PADS_2	Generic PIO
7	PIO13	DI/DO	VDD_PADS_2	Generic PIO
13	PIO14	DI/DO	VDD_PADS_2	Generic PIO
17	PIO15	DI/DO	VDD_PADS_2	Generic PIO
15	PIO16	DI/DO	VDD_PADS_2	Generic PIO
19	PIO17	DI/DO	VDD_PADS_2	Generic PIO
21	PIO18	DI/DO	VDD_PADS_2	Generic PIO
23	PIO19	DI/DO	VDD_PADS_2	Generic PIO
25	PIO20	DI/DO	VDD_PADS_2	Generic PIO
36	PIO21	DI/DO	VDD_PADS_2	Generic PIO
32	PIO22	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable
30	PIO23	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable
34	PIO24	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable
27	PIO25	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable

2.2.3 IO Pin Mux Table

GPIO	QSPI	I2C	FTC	LED	Analog	CoEx	Debug	SE0	SE1	SE2	SE3
PIO0	QSPI_CLK	SDA	ftc0_out	BLUE				Port 0	Port 0	Port 0	Port 0
PIO1	QSPI_MOSI	SCL	ftc0_out	RED				Port 1	Port 1	Port 1	Port 1
PIO2	QSPI_MISO	SDA	ftc0_out	GREEN				Port 2	Port 2	Port 2	Port 2
PIO3	QSPI_CSB	SCL	ftc1_out	WHITE				Port 3	Port 3	Port 3	Port 3
PIO4	QSPI_IO2	SDA	ftc1_out	WHITE				Port 0	Port 4	Port 4	Port 4
PIO5	QSPI_IO3	SCL	ftc1_out	BLUE				Port 1	Port 0	Port 0	Port 0
PIO6		SDA	ftc_in	RED				Port 2	Port 1	Port 1	Port 1
PIO7		SCL		GREEN				Port 3	Port 2	Port 2	Port 2
PIO8								Port 4	Port 3	Port 3	Port 3
PIO9							TCK/SWD_CLK		Port 4	Port 4	Port 4
PIO10							TMS/SWD_DIO		Port 0	Port 0	Port 0
PIO11	QSPI_CLK	SDA	ftc_in				TDI/test_hf	Port 0	Port 1	Port 1	Port 1
PIO12	QSPI_MOSI	SCL					TDO/SWO	Port 1	Port 2	Port 2	Port 2
PIO13	QSPI_MISO	SDA	ftc2_out				Test_lf	Port 2	Port 3	Port 3	Port 3
PIO14	QSPI_CSB	SCL	ftc2_out					Port 3	Port 4	Port 4	Port 4
PIO15	QSPI_IO2	SDA	ftc2_out	BLUE/WHITE			trace_ctrl	Port 4		Port 3	Port 3
PIO16	QSPI_IO3	SCL	ftc_in	RED/WHITE			trace_clk	Port 0	Port 0	Port 1	Port 1
PIO17		SDA	ftc3_out	GREEN/WHITE			trace_data_0	Port 1	Port 1	Port 2	Port 2
PIO18		SCL	ftc3_out	WHITE			trace_data_1	Port 2	Port 2	Port 3	Port 3
PIO19		SDA	ftc3_out	WHITE			trace_data_2	Port 3	Port 3	Port 4	Port 4
PIO20		SCL		WHITE		slv_pta_coex_active	trace_data_3	Port 4	Port 4		
PIO21		SDA	ftc_in	WHITE		slv_pta_coex_status		Port 0	Port 0	Port 0	Port 0
PIO22		SCL		BLUE	ADC	slv_pta_coex_confx		Port 1	Port 1	Port 1	Port 1
PIO23		SDA		RED	ADC	mstr_pta_coex_active		Port 2	Port 2	Port 2	Port 2
PIO24		SCL		GREEN	ADC	mstr_pta_coex_status		Port 3	Port 3	Port 3	Port 3
PIO25				WHITE	ADC	mstr_pta_coex_confx		Port 4	Port 4	Port 4	Port 4

2.2.4 Programmable Series Engine

Serial Engines (SE) and supported interfaces

SE	3-wire or 4-wire SPI Display Controller	True 4-wire SPI Controller/Peripheral	I2C Controller	8-bit UART	9-bit UART
SE0	Yes	Yes	Yes	Yes	Yes
SE1	Yes	Yes	Yes	Yes	Yes
SE2	-	-	Yes	Yes	-
SE3	-	-	Yes	Yes	-

Serial engines default port mappings

SE	3-wire Display	4-wire Display	I2C	UART	SE0 true 4-wire SPI
Port 0	CS1	CS1	SDA	CTS	MISO
Port 1	SDIN	SDIN	SCL	RTS	MOSI
Port 2	CLK	CLS	-	TXD	CLS
Port 3	CS	CS	-	RXD	CS
Port 4		D/C	-	-	CS1

2.3 Computing Subsystem

2.3.1 Microcontroller

EQM100-5 modules have Qualcomm QCC711 at his core which integrates three microcontrollers – Arm Cortex-M3 processor, Arm Cortex-M0 processor, and RISC-V:

Arm Cortex-M3 processor – Running at 32MHz, dedicated to higher layer protocol and user applications. It conducts inter-processor communication with Arm Cortec-M0 processor for BLE services and with RISC-V processor for security services.

Arm Cortex-M0 processor – Running at 32MHz, dedicated to BLE radio and lower protocol layer (MAC) processing.

RISC-V processor – Running at 32MHz, dedicated to security services. it can function as a Root-of-Trust (RoT) processor to execute highly secure bootup code under Trusted Execution Environment (TEE) that validate the user application image before handing over the control to Arm Cortex-M3 processor. RISC-V has its own 32KB SRAM, 192KB ROM and protected OTP area and will be NOT visible to user applications, making it highly reliable and secure.

The computing subsystem software architecture consists of three parts as illustrated below. Computing Subsystem (APSS) will be open-sourced on GitHub while Bluetooth Subsystem (BTSS) and Security Subsystem will be offered binary inside software SDK package.

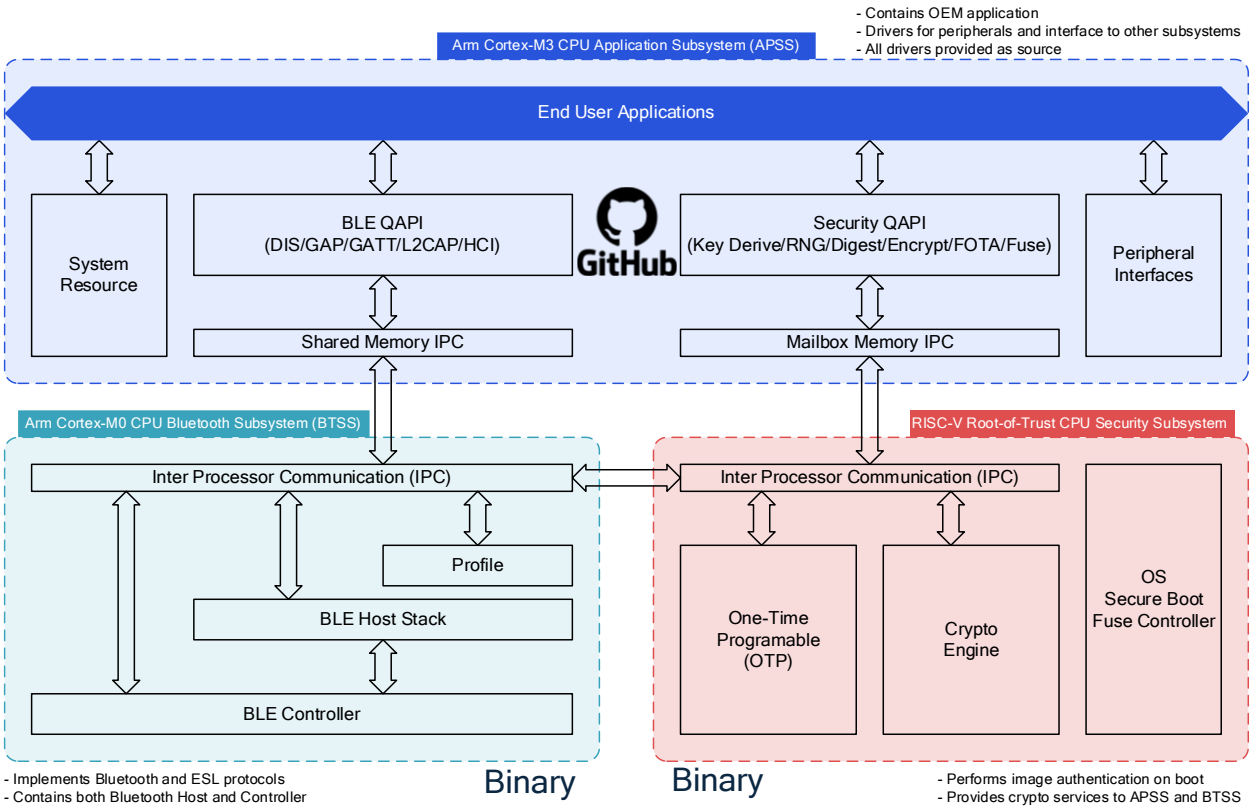

Figure 8: Computing subsystem software architecture

2.4 Memory

There are 512KB on-chip RRAM, 128KB on-chip SRAM and 2KB OTP/MTP shared among three processors. Built-in Non-volatile memory RRAM hosting execution code will eliminate needs of an external NOR flash to reduce system cost. 416KB out of 512KB RRAM can be used for user applications. 128KB SRAM can be used for runtime data. 64KB out of 128KB SRAM can be used for user applications.

Additional NOR flash can be added through QSPI interface for additional data storage.

2.5 Peripheral Interfaces

EQM100-5 modules supports the following peripheral interfaces through 26x configurable PIO:

- 2x SPI master or slave, support 3-wire/4-wire SPI for display and true 4-wire SPI with DMA
- 2x I2C master and 1x I2C slave, supporting 100kbps, 400kbps, and 1000kbps data rate
- 3x UART with hardware flow control, supporting maximum 2M baud rate
- 4x 10-bit ADC (1.8V only)
- 4x FTC (PWM)
- 3-wire PTA coexistence master or slave
- SWD with 4-bit trace

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

The absolute maximum ratings provided in this section reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating.

Pin	Parameter	Min	Max	Unit
VDD_VBATT	Power input voltage	VDD_PADS_2	3.63	V
VDD_PADS_1	I/O port 1 voltage	VSS - 0.3	3.63	V
VDD_PADS_2	I/O port 2 voltage	VSS - 0.3	3.63	V
Digital I/O	PIO25:PIO9	VSS - 0.3	VDD_PADS_2 + 0.3	V
	PIO8:PIO0	VSS - 0.3	VDD_PADS_1 + 0.3	V
	MFP	VSS - 0.3	VDD_VBAT + 0.3	V
All ground / VSS pads		0	0	V
Storage temperature		-40	85	°C

3.2 Recommended Operating Conditions

Pin	Parameter	Min	Max	Unit
VDD_VBATT	Power input voltage	1.71	3.6	V
VDD_PADS_1	I/O port 1 voltage	0	3.6	V
VDD_PADS_2	I/O port 2 voltage	0	3.6	V
Digital I/O	PIO25:PIO9	VSS	VDD_PADS_2	V
	PIO8:PIO0	VSS	VDD_PADS_1	V
	MFP	VSS	VDD_VBAT	V
All ground / VSS pads		0	0	V
Storage temperature		-40	85	°C

4 Radio Performance

Channel Bandwidth	Modulation	Parameter	Data Rate	Typical	Unit
2MHz	GFSK	Tx Power	2Mbps	+6	dBm
			1Mbps	+6	dBm
			500kbps	+6	dBm
			125kbps	+6	dBm
		Rx Sensitivity @ 30.8% PER (Boost Mode)	2Mbps	-93	dBm
			1Mbps	-96	dBm
			500kbps	-98	dBm
			125kbps	-103	dBm
		Rx Sensitivity @ 30.8% PER (Normal Mode)	2Mbps	TBD	dBm
			1Mbps	TBD	dBm
			500kbps	TBD	dBm
			125kbps	TBD	dBm
Note: VDD_VBAT = 3.3V					

5 Power Consumption

EMQ100-1 modules can operate in four power states as shown below to maximize power saving:

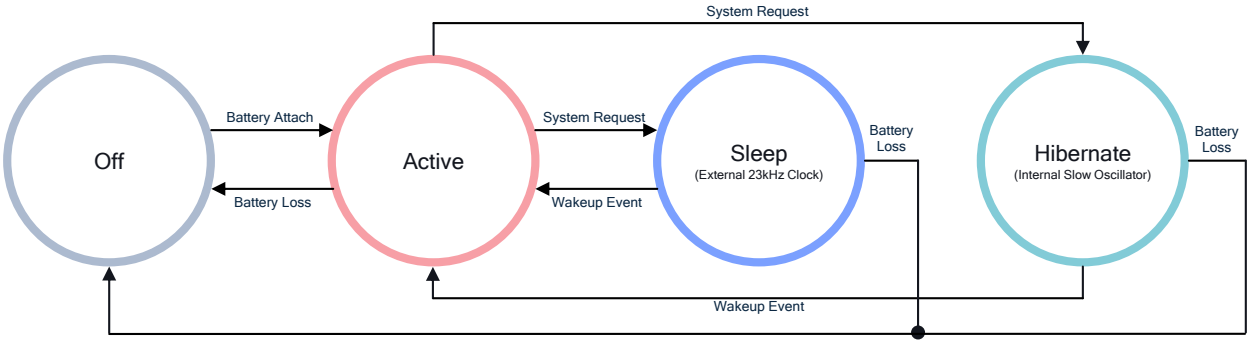

Figure 9: Power State Diagram

5.1 Active Power

Channel Bandwidth	Modulation	Parameter	dBm	Average Current	Unit
2MHz	GFSK	Tx Power	0	10.5	mA
			+4	14.6	mA
			+6	16.6	mA
		Rx Power Normal	TBD	TBD	mA
		Rx Power Boost	-95	5.3	mA

5.2 Sleep Power

Test Mode	MCU State	Average Current	Unit
• Software controlled • 16KB SRAM retained • 32kHz crystal running • Measured from the SDK - once connected to an AP	Sleep	4	µA
• Software controlled • No SRAM retained • Internal LFLPO running • Measured from the SDK - not connected to an AP	Hibernate	16	µA

6 Mechanical Specification

6.1 U.FL Antenna

6.1.1 Dimension

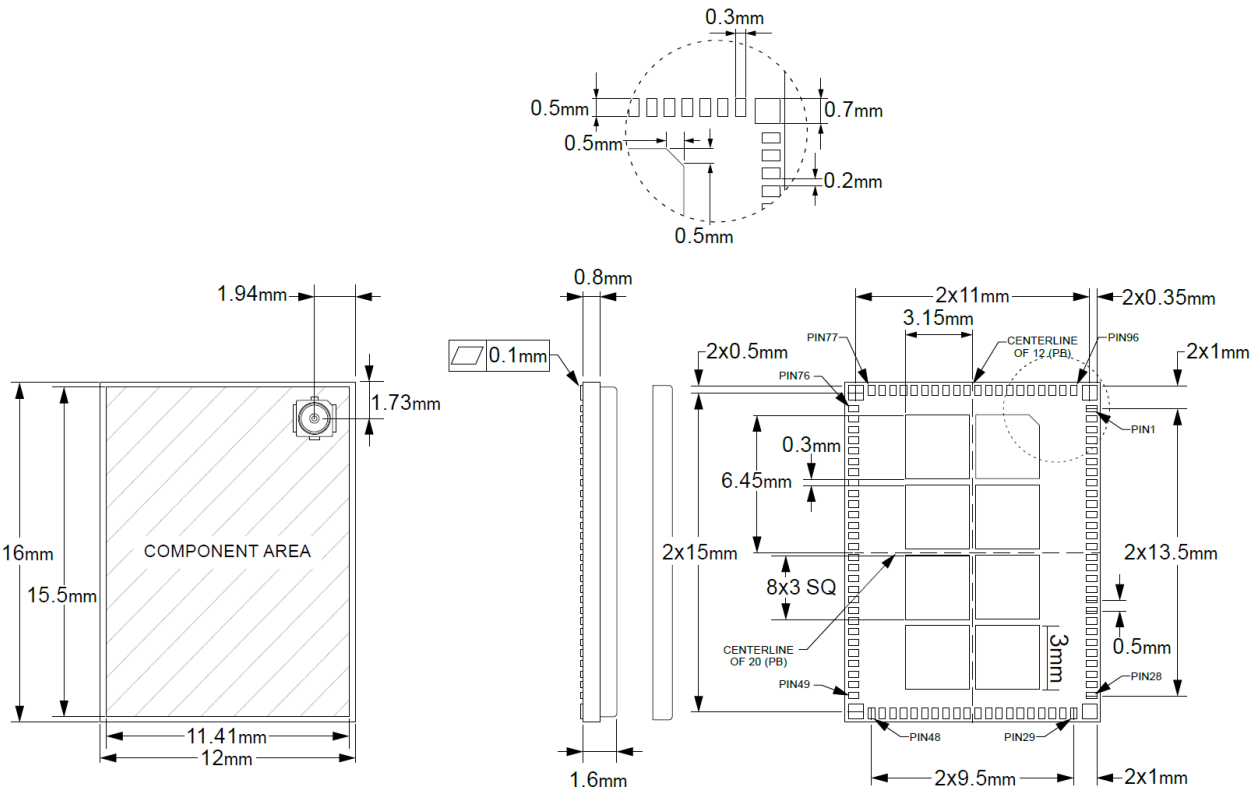

Figure 10: EMQ100-5U Dimension

6.1.2 Recommended PCB Landing Pattern

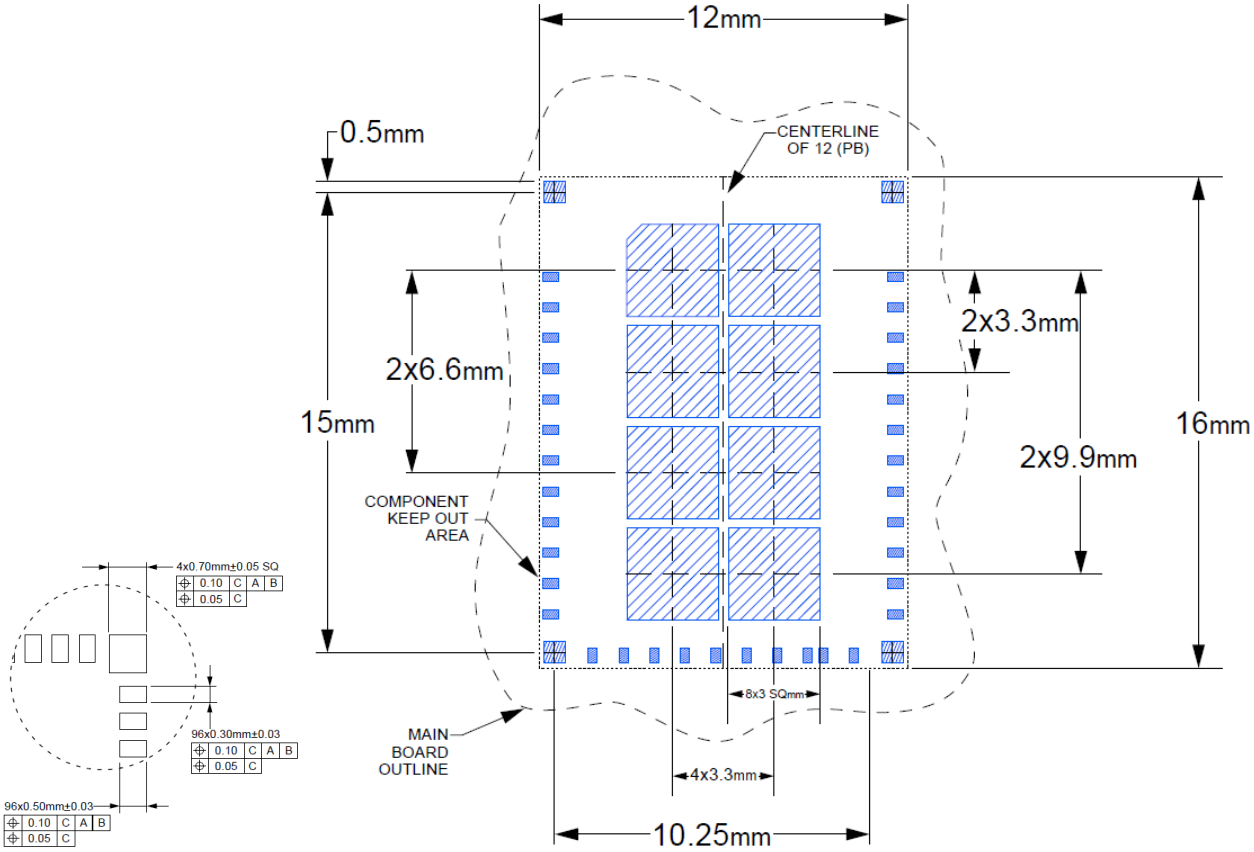

Figure 11: EMQ100-5U PCB Landing Pattern

6.2 PCB Antenna

6.2.1 Dimension

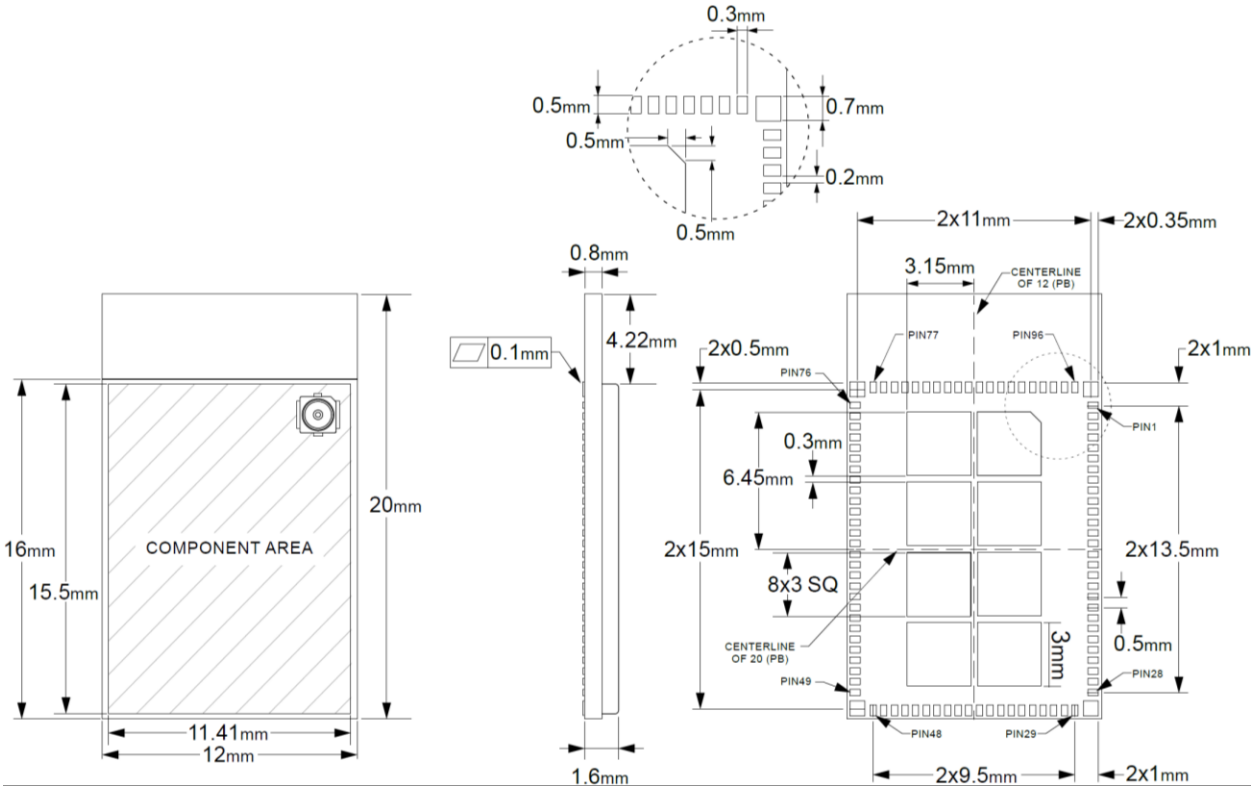

Figure 12: EMQ100-5B Dimension

6.2.2 Recommended PCB Landing Pattern

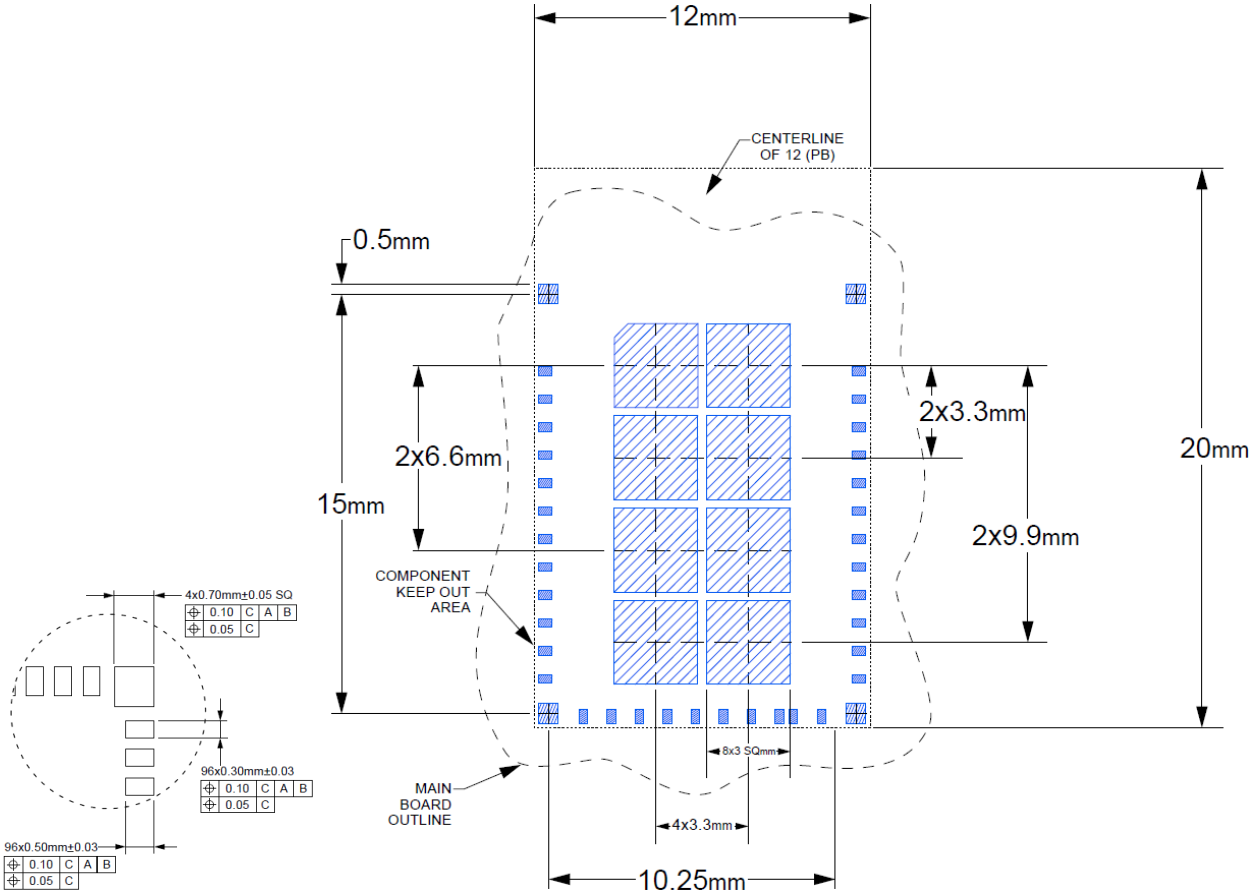

Figure 13: EMQ100-5B PCB Landing Pattern

7 Manufacturing Recommendation

7.1 Power Layout Guideline

EQM100-5 modules are powered by either 3V battery or DC 3.3V. Power pin connection capacitor is as close as possible to chip and pin. Decoupling the power supply from the chip using a capacitor. Use capacitors to prevent noise from coupling back to the power plane.

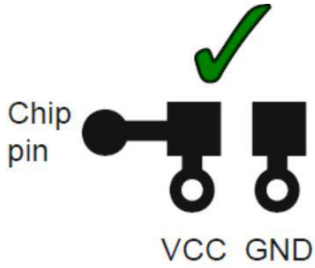

Figure 14: Power Layout Guideline

7.2 RF Layout Guideline

To optimize antenna performance, place the module in the corner of the PCB as shown below. Do not cover copper and trace the antenna clearance area. Keep the antenna area as far away as possible from the power supply and metal components. Connect all GND pins directly to a solid GND plane. Place GND vias as close as possible to the GND pin. Use a good layout method to avoid excessive noise coupling with signal lines or supply voltage lines.

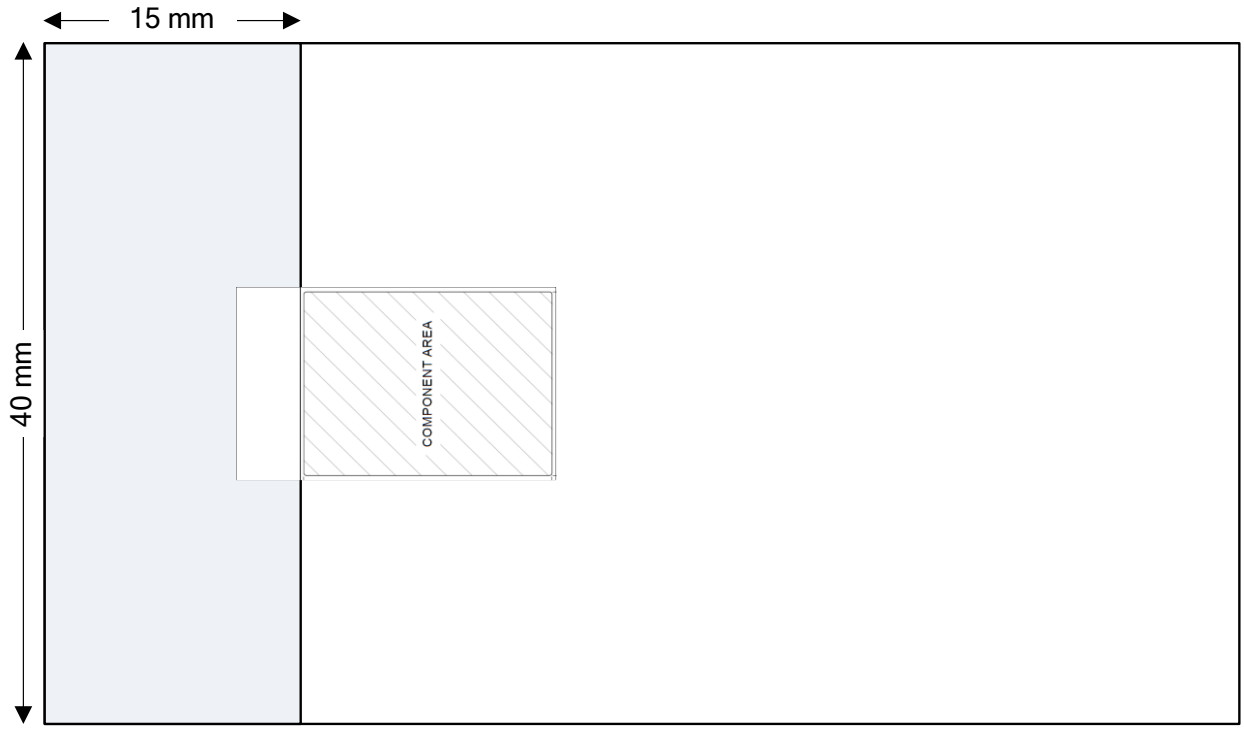

Figure 15: RF Layout Guideline

7.3 Soldering Recommendations

EQM100-5 modules can be SMT on the board following the temperature curve graph:

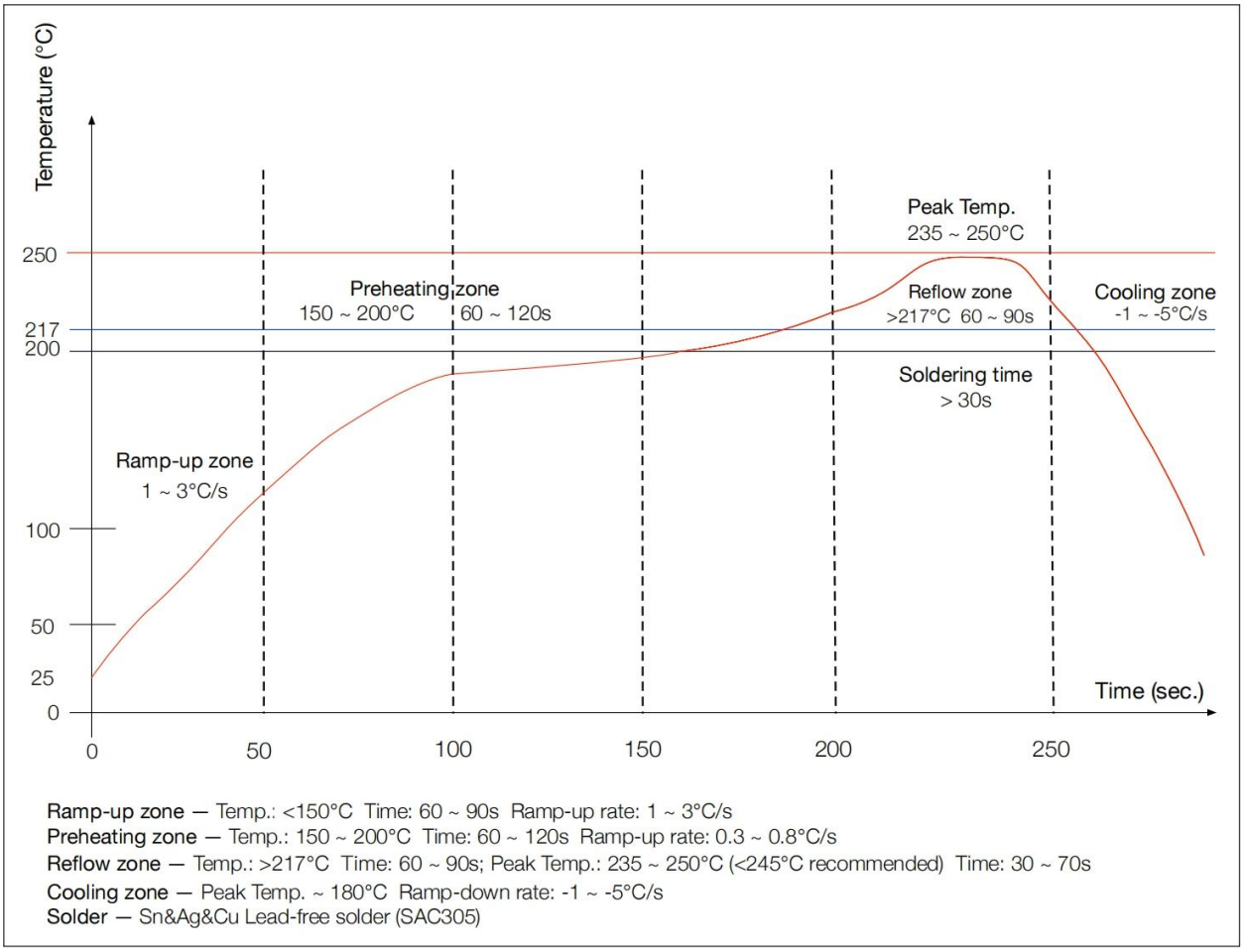

Figure 16: Soldering Guideline

8 Packaging

EQM100-5 modules are packaged on reels loaded with 1000 modules. Each reel is placed in an antistatic bag with a desiccant pack and a humidity card and placed in an 36x25x12cm box. Anti-static warnings and labels adhere to the outside of the bag.

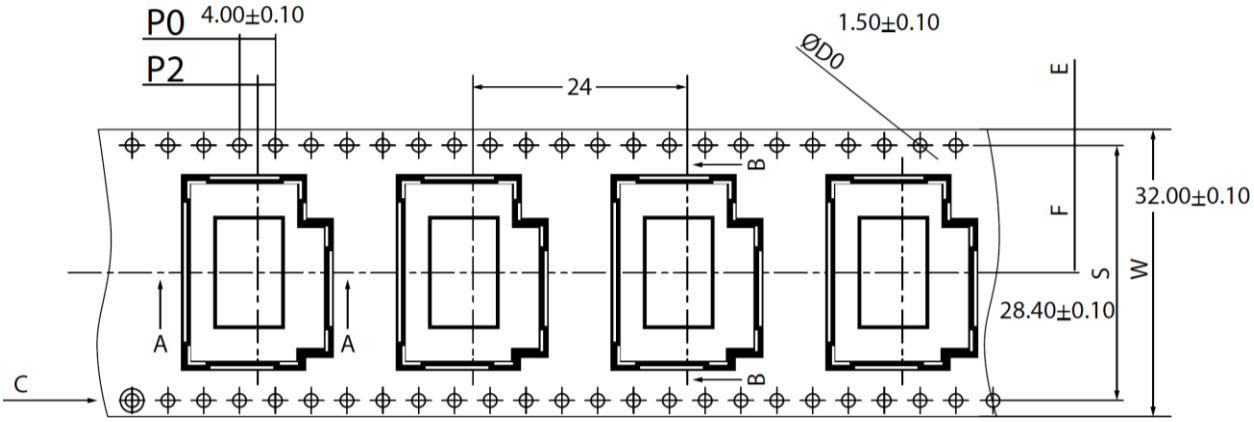

Figure 16: Module Packaging

Warning

The MeshConnect Modules contain highly sensitive electronic circuitry. Handling without proper ESD protection may destroy or damage the module permanently.

Warning

The MeshConnect Modules are moisture-sensitive devices. Appropriate handling instructions and precautions are summarized in J-STD-033. Read carefully to prevent permanent damage due to moisture intake.

Moisture Sensitivity Level (MSL)

EQM100-5 is qualified to moisture sensitivity (MSL3) in accordance with JEDEC J-STD-020

Storage

Storage/shelf life in sealed bags is 12 months at <40°C and <90% relative humidity.12.2 Packing Label

9 Regulatory Compliance

Country	Certification	No
USA	FCC 15C	TBD
Europe Union	CE	TBD
Canada	IC	TBD
Japan	MIC	TBD
Korea	KC	TBD
Australia	RCM	TBD
United Kingdom	UKCA	TBD
China	SRRC	TBD

10 Order Information

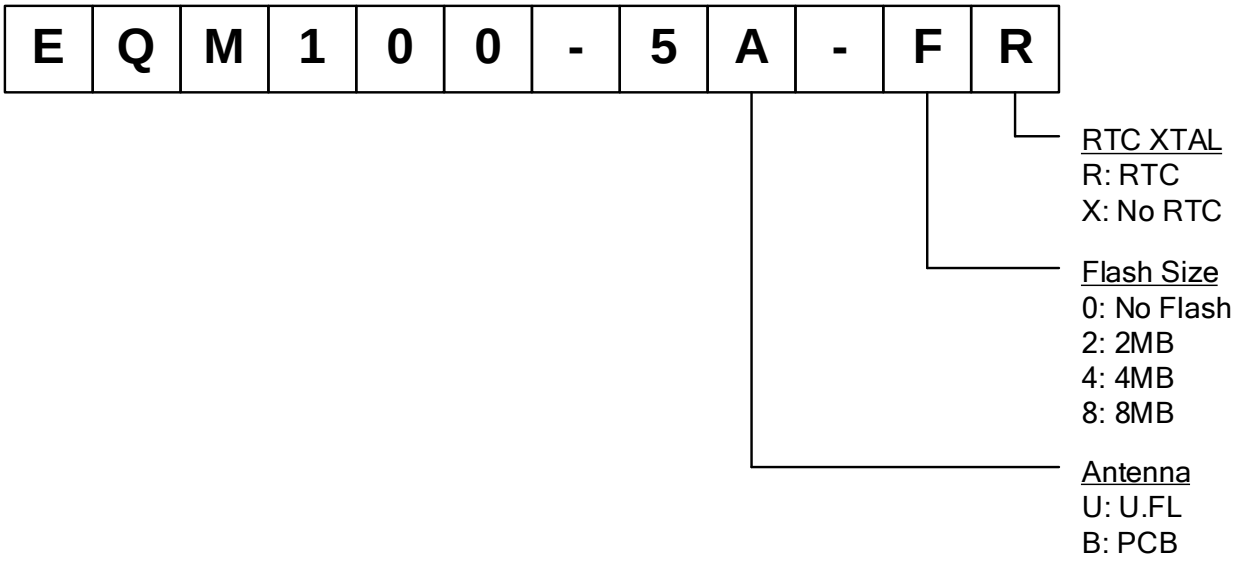

Figure 18: Ordering Part Number

Revision History

Revision	Description	Date
0.1	Initial draft	August 15, 2023
1.0	The first public release	TBD

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